METHOD FOR MANUFACTURING HIGH Tc SUPERCONDUCTING CIRCUIT ELEMENTS WITH METALLIC SUBSTRATE

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ABSTRACT

A method for manufacturing a high Tc superconducting circuit elements is disclosed, which comprises the steps of preparing a single crystal conductive substrate of Sr₂RuO₄ by a floating zone melting process; epitaxially growing on the (001) surface of the Sr₂RuO₄ substrate a high Tc copper oxide-based superconducting film with a thickness of 1 to 1000 nm; depositing metal pads onto said superconducting film to form electrical contacts; and applying a metal pad to the surface of the substrate to form an electrical contact.

10 Claims, 2 Drawing Sheets
METHOD FOR MANUFACTURING HIGH $T_c$ SUPERCONDUCTING CIRCUIT ELEMENTS WITH METALLIC SUBSTRATE

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BACKGROUND

This invention relates to superconducting circuit elements, namely heterostructures such as SNS Josephson junctions and field-effect transistors, having a sandwich structure consisting of at least one layer of high-$T_c$ superconductor material arranged adjacent to a metallic substrate, having an insulating layer interposed between the high-$T_c$ material and the metallic substrate. Both the substrate and the insulator consist of materials having structural properties sufficiently similar to those of the superconductor so that mechanical and chemical compatibility is guaranteed.

For device applications of high-$T_c$ superconductors, it is desirable to find electrically conductive materials, in particular metals, which are compatible with the high-$T_c$ superconductor materials. Compatibility in this context means a best possible match of the respective lattice constants, and the absence of deleterious diffusion effects at the interfaces of the materials involved. These materials may be used, for example, in thin film form for SNS heterostructures (where S stands for superconductor, and N stands for normal metal), or they may serve as the bulk substrate in a field-effect transistor among other applications.

European application EP-A-0 409 338 discloses a planar Josephson device of the type where at least one layer of non-superconducting material is arranged between two layers of a superconductor material in one embodiment described, the superconductor is YBa$_2$Cu$_3$O$_{7-8}$ and the non-superconductor is silver sulphate Ag$_2$SO$_4$. The silver sulphate being connected to the superconductor through layers of silver which serve to prevent diffusion of the sulphate into the superconductor.

The existence of an electrical field-effect in copper oxide high-$T_c$ superconductors (although later found to be very small) has already been reported by U. Kabasawa et al. in Japanese Journ. of Appl. Phys. 29 L86, 1990, and EP-A-0 324 044 actually describes a three-terminal field-effect device with a superconducting channel. Electrical fields are used to control the transport properties of channel layers consisting of high-$T_c$ superconductor material. While this seemed to be a promising approach, growth studies of such devices have shown that in the suggested configuration, the ultrathin superconducting layers readily degrade during deposition of insulator layer and top electrode.

The lattice constant matching problem has been tackled by using doped and undoped versions of the same material. In particular, the substrate, is used as the gate electrode of a field-effect transistor of the MISFET type. The substrate consists of conducting niobium-doped strontium titanate. On that substrate, a barrier layer consisting of undoped strontium titanate is epitaxially grown, and onto the latter the current channel layer consisting of the superconducting YBa$_2$Cu$_3$O$_{7-8}$ is epitaxially deposited. It has been found (cf. H. Hagesawa et al., Jap. Journ. Appl. Phys., Vol. 28 (1989)L2210) that during film growth a thin insulating surface layer forms on the Nb-doped SrTiO$_3$, reducing the sensitivity of the device. The formation of this layer is possible due to a diffusion of Nb atoms from the gate/insulator interface into the bulk of the gate electrode.

SUMMARY OF THE INVENTION

It is an object of the present invention to overcome these disadvantages of the prior art. In accordance with the invention, metallic strontium ruthenate (or strontium ruthenium oxide) Sr$_2$Ru$_2$O$_7$ is used as substrate material for the high-$T_c$ superconductor and circuit elements formed from the high-$T_c$ superconductor. These superconducting circuit elements, namely SNS heterostructures, such as, e.g. Josephson junctions and field-effect transistors, have a sandwich structure consisting of at least one layer of high-$T_c$ superconductor material arranged adjacent to a metallic substrate, possibly with an insulating layer in between, the substrate, the superconductor and if present the insulator all consisting of materials having at least approximately matching molecular structures and lattice constants. Electrical contacts, such as source, drain and gate electrodes are attached to the superconductor layer and to the substrate, respectively. The electrically conductive substrate consists of a metallic oxide such as strontium ruthenate Sr$_2$Ru$_2$O$_7$, whereas the superconductor layer is of the copper oxide type and may be YBa$_2$Cu$_3$O$_{7-8}$, for example. The insulator layer may consist of SrTiO$_3$. The manufacture of these devices starts with the preparation of the substrate material from a 2:1:1 molar ratio of SrCO$_3$ to RuO$_2$ and involves a floating zone melting process yielding single crystals of the strontium ruthenate Sr$_2$Ru$_2$O$_7$ material onto whose (001) surface the superconductor layer as well as the barrier layer can be epitaxially deposited.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 shows the resistivity $\rho(T)$ versus temperature characteristic of Sr$_2$Ru$_2$O$_7$.

FIG. 2 is a diagram showing the resistance of a YBa$_2$Cu$_3$O$_{7-8}$ film grown on a Sr$_2$Ru$_2$O$_7$ substrate in dependence on temperature;

FIG. 3 shows an SNS heterostructure with a Sr$_2$Ru$_2$O$_7$ substrate;

FIG. 4 is an inverted MISFET structure using a Sr$_2$Ru$_2$O$_7$ substrate;

FIG. 5 shows essentially the device of FIG. 4 with a supporting layer.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The prior art problem of undesired surface layers on the Nb-doped SrTiO$_3$ can be avoided if substrates are used as gate electrodes which are intrinsically metallic and that do not rely on dopants to induce metallic behavior. However, the intrinsically metallic substrate must be compatible with the high-$T_c$ superconductor material.

Most of the high-$T_c$ superconductor materials known today have very similar molecular structures and essentially the same lattice constants. Examples of high-$T_c$ superconductors of the copper oxide type which can be used in connection with the present invention are listed in the table below, together with the respective reference where a description can be found:

<table>
<thead>
<tr>
<th>Superconductor Composition</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti-Ba-Ca-Cu-O</td>
<td>EP-A-0 332 309</td>
</tr>
</tbody>
</table>
In addition to the high-\(T_c\) copper oxide superconductor materials of which examples are listed above, there are some other high-\(T_c\) superconductor materials known which do not rely on copper but other elements, such as bismuth, for example. On such material in \(\text{Ba}_2\text{K}_8\text{Cu}_4\text{O}_{9}\delta\) which was described by R. J. Cava et al., “Superconductivity Near 30 K Without Copper: The \(\text{Ba}_2\text{K}_8\text{Cu}_4\text{O}_{9}\delta\)” Nature, Vol. 332, No. 6167, pp. 814–816 (1988). The common characteristic of all known high-\(T_c\) superconductor materials which may be used in connection with the invention is that they have a perovskite or perovskite-related structure.


Without intending to be restrictive, the description of the invention given below will use \(\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}\) (with \(0 \leq \delta \leq 1\)) as an example of a high-\(T_c\) superconductor material, with the understanding that any other high-\(T_c\) superconductor material can be used instead, provided its molecular structure and lattice constants are sufficiently close to those of strontium ruthenate \(\text{Sr}_2\text{RuO}_4\), and this is the case at least with all known high-\(T_c\) copper oxide superconductors and the bismuth oxide compound mentioned above.

In accordance with the present invention, the disadvantages of the prior art are overcome by superconducting circuit elements having a multilayered structure, comprising at least one layer of a high-\(T_c\) superconductor material arranged adjacent to a substrate consisting of a metallic conductor material having a molecular structure and lattice constants which are the greatest distance apart of those of said high-\(T_c\) superconductor material, the circuit elements being characterized in that said high-\(T_c\) superconductor material is of the perovskite-related type and that said electrically conductive substrate consists of strontium ruthenate \(\text{Sr}_2\text{RuO}_4\).

The existence of \(\text{Sr}_2\text{RuO}_4\), as a bulk material and a\(\delta\), is already known from reports by J. J. Randall et al., “The Preparation of Some Ternary Oxides of the Platinum Metals”, J. Am. Chem. Soc. Vol. 81 (1959) pp. 2629–2631, and by A. Callaghan et al., “Magnetic Interactions in Ternary \(\text{RuO}_2\) Oxides”, Inorganic Chem., Vol. 5, No. 9 (1966) pp. 1572–1576. Of course, at the time of these reports, the high-\(T_c\) copper oxide superconductor materials were still unknown. Single-crystals of \(\text{Sr}_2\text{RuO}_4\) were grown for the first time by the inventors and revealed a highly conductive metallic in-plane behavior which was not before known from the ceramic \(\text{Sr}_2\text{RuO}_4\) bulk material.

The method for manufacturing superconducting circuit elements in accordance with the invention is characterized by the following steps:

1. Weighing appropriate ratios of strontium carbonate \(\text{SrCO}_3\) and ruthenium dioxide \(\text{RuO}_2\), and grinding;
2. Mixing the powder with water and pressing it to form two rods;
3. Sintering the rods in air at a temperature of about 1300°C;
4. Melting the rods in air in a floating zone melting process;
5. Growing samples from the melt having cylindrical shape with layers (a-b-planes) of strontium ruthenate \(\text{Sr}_2\text{RuO}_4\) along the axis of the cylinder;
6. Cleaving the melt-grown samples to obtain single-crystal substrates having defined crystallographic surfaces;
7. Rinsing the substrate in a cleaning solvent;
8. Attaching the single crystal to the heater of a sputtering chamber and sputtering with the following parameters:
   - substrate heater block temperature: 700°–750°C;
   - total pressure \(\text{Ar}/\text{O}_2 = 2:1\): 0.845 mbar;
   - plasma discharge: 150–170 V, 450 mA;
   - aftergrowth cooldown in \(\propto 0.5\) bar \(\text{O}_2\) lasting for about 1 hour;
9. Epitaxially growing on at least one (001)-surface of the \(\text{Sr}_2\text{RuO}_4\) substrate a film of a high-\(T_c\) superconducting material, with the thickness of the superconductor film being in the range of 1 to 1000 nm;
10. Depositing metal pads onto the superconductor layer(s) to form electrical contacts;
11. Applying a metal pad to the surface of the substrate facing away from said superconducting layer to form an electrical contact.

Details of three embodiments of the invention will hereafter be described by way of example and with reference to the drawings in which:

- FIG. 1 shows the resistivity \(\rho\) versus temperature characteristic of \(\text{Sr}_2\text{RuO}_4\);
- FIG. 2 is a diagram showing the resistance of a \(\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}\) film grown on a \(\text{Sr}_2\text{RuO}_4\) substrate in dependence on temperature;
- FIG. 3 shows an SNS heterostructure with a \(\text{Sr}_2\text{RuO}_4\) substrate;
- FIG. 4 is an inverted MISFET structure using a \(\text{Sr}_2\text{RuO}_4\) substrate;
- FIG. 5 shows essentially the device of FIG. 4 with a supporting layer.

A metallic substrate is highly desirable for thin film applications of high-\(T_c\) superconductor materials, such as, e.g., \(\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}\), for a number of reasons: It can be used as a gate electrode in a field-effect device. It can be used as a shunt resistance. It has a high thermal conductivity than \(\text{SrTiO}_3\) and, therefore, allows denser packaging of the devices. It offers a convenient electrical contact from the superconductor to the external world or to other devices.

The problem with the metals and alloys so far considered for use in connection with high-\(T_c\) superconductor materials is simply that none of them has a lattice that matches the lattice structure of the superconductor material in question to any useful extent. Also, in some cases, diffusion across the interface between the materials tends to destroy the ability to become superconducting. Accordingly, none of these metals has found an
application together with a high-$T_c$ superconductor, except, perhaps as a contact material.

In a contrast, the paramagnetic Sr$_2$RuO$_4$ has a layered $K_2NiF_4$-structure and is a metallic conductor along its layers, with an excellent lattice match to copper oxide superconductors, such as YBa$_2$Cu$_3$O$_{7-\delta}$. At 300 K, Sr$_2$RuO$_4$ is tetragonal with lattice constants of $a=b=0.387$ nm, and $c=1.274$ nm, as compared to YBa$_2$Cu$_3$O$_{7-\delta}$ which is orthorhombic with lattice constants of $a=0.382$ nm, $b=0.389$ nm, and $c=1.17$ nm. This small lattice mismatch (of about 1.3%) compares favorably even to that between YBa$_2$Cu$_3$O$_{7-\delta}$ (001) and strontium titanate SrTiO$_3$[100], the latter being the standard insulating substrate for the growth of superconducting copper oxides, and which at 300 K is cubic, with $a=0.391$ nm (as shown in EP-A-0 324 220).

FIG. 1 shows the resistivity $\rho$-versus-temperature characteristic measured at a representative Sr$_2$RuO$_4$ crystal. No corrections for inhomogeneous current density distribution had to be made. In the a-b-plane, the resistivity ranges from $\rho_{ab}=10^{-4}\Omega\text{cm}$ at room temperature down to $\rho_{ab}=10^{-6}\Omega\text{cm}$ at 4.2 K demonstrating the highly conductive metallic in-plane behavior of Sr$_2$RuO$_4$. The observed resistivity along the c-axis resembles that of the layered materials TaS$_2$ and graphite. Like Sr$_2$RuO$_4$, they exhibit a metallic behavior along the layers and a resistivity maximum between room temperature and 4.2 K perpendicular to the layers.

Generally, when it is possible to grow Sr$_2$RuO$_4$ on SrTiO$_3$ and vice-versa, thin film devices become feasible where insulating, superconducting and metallic layers can be combined in any way.

To demonstrate their compatibility, thin films of YBa$_2$Cu$_3$O$_{7-\delta}$ were grown onto the a-b-plane of a Sr$_2$RuO$_4$ crystal with very satisfactory results. The diagram of FIG. 2 shows the resistance of such a film in dependence on the temperature, with a critical temperature $T_c$ of 86 K.

Referring now to FIG. 3, there is shown an SNS heterostructure 1 comprising an electrically conducting Sr$_2$RuO$_4$ crystal forming a substrate 2 and carrying on both sides thin-film superconductor layers 3 and 4 consisting of YBa$_2$Cu$_3$O$_{7-\delta}$. As mentioned above, the lattice constants of the substrate material match the lattice constants of the superconductor material to such an extent that epitaxial growth of the superconductor films 3, 5 onto the substrate 2 is possible without a problem. Contact terminals 5 and 6 are attached to superconductor layers 3 and 4, respectively.

FIG. 4 shows a field-effect transistor 7 having an inverted MISFET-structure. In this structure, a superconducting YBa$_2$Cu$_3$O$_{7-\delta}$ film 8 of the thickness $s$ is separated from a Sr$_2$RuO$_4$ crystal substrate 9 serving as a gate electrode, by an insulating SrTiO$_3$ barrier layer 10 of the thickness $t$. Besides the thickness $s$ of the superconductor film 8, the resistivity $\rho_t$ and the breakdown field strength $E_{BD}$ of the insulator layer 10 are crucial parameters. The required values for $E_{BD}$ and for $\rho_t$ can be simply estimated, if space charge effects are neglected: To induce a surface charge density in superconducting film 8 which corresponds to the unperturbed density $n$ of mobile charge carriers ($n\delta^3 \ldots 5 \times 10^{21}/\text{cm}^3$), the capacitor formed by substrate 9 and superconductor film 8 has to be biased with a voltage $V_0 = \frac{en}{\epsilon_0}$.

where $q$ is the elementary charge, $\epsilon_0$ and $\epsilon_r$ respectively the dielectric constants of the vacuum and of the barrier layer material. Equation (1) rewritten provides the condition for the breakdown field strength $E_{BD}$:

$$E_{BD} \geq \frac{V_0}{t} = \frac{en}{\epsilon_0\epsilon_r}$$

Equation (2) implies that to modulate the carrier density $n$ in high-$T_c$ superconductors substantially, the product $\epsilon_r E_{BD}$ has to be of the order of $10^8$ V/cm. (For comparison, SiO$_2$ has an $\epsilon_r E_{BD}$ product of $4 \times 10^7$ V/cm at room temperature.) In addition, the normal-state resistivity $\rho_t$ of the insulator has to be sufficiently high to avoid leakage currents which result in an input loss $\frac{V_G}{\lambda_G}$, the latter factor being the gate current. For a typical case of $\lambda_G < 1\mu m$, $1\mu m = 10\mu A$, and an area of the substrate 9 of 1mm$^2$, the resistivity $\rho_t$ must be higher than $10^{14}$ ohm$cm/\epsilon_r$ at operating temperature.

In view of these requirements, insulating layers with high dielectric constants are recommended. Therefore, SrTiO$_3$ is a good material for insulating barrier layer 10 because of its good compatibility with the growth of copper oxide superconductors, such as YBa$_2$Cu$_3$O$_{7-\delta}$. The compatibility of YBa$_2$Cu$_3$O$_{7-\delta}$ with SrTiO$_3$ has already been pointed out in EP-A-0 299 870 and EP-A-0 301 646.

The dielectric constant $\epsilon_r$ of SrTiO$_3$ being between 40 and 300 (depending on the purity of the material), the breakdown field being on the order of $10^5$ V/cm, and with an operating voltage $V_G=5V$, equation (2) suggests that a monomolecular (i.e. unit cell) layer of superconductor material would meet the requirements. Accordingly, with $s=1.2$ nm and $n_{32} 260$ and a carrier density $n_{32} 3 \times 10^{11}$ cm$^{-2}$, equation (1) yields a value of $\lambda_G = 20$ nm.

The manufacture of the Josephson junction heterostructure of FIG. 3 and of the inverted MISFET device in accordance with FIG. 4 preferably involves the following steps:

1. Appropriate ratios, molar ratios, for example, of strontium carbonate SrCO$_3$ and ruthenium dioxide RuO$_2$ are weighed with an accuracy of better than 1%/0.

2. After grinding, the powder is mixed with water and pressed to form rods of, say, 5 mm diameter, one 10 mm in length, the other 100 mm in length, for example.

3. The rods are sintered on Al$_2$O$_3$ boats in air at about 1300°C.

4. Using the floating zone process, the rods are melted in air in a mirror cavity with focused infrared radiation, the short rod being used as the seed, the long rod being used as the feed material.

5. Single-crystals are grown from the melt. The melt-grown samples have cylindrical shape with layers (a-b-planes) of Sr$_2$RuO$_4$ grown along the axis of the cylinder.

The growth of the Sr$_2$RuO$_4$ crystals is complicated by the volatility of RuO$_2$ which leads to the segregation of SrO. To compensate for this segregation, an excess of RuO$_2$ must be used in the starting material. A molar ratio of 2:1:1 of SrCO$_3$ and RuO$_2$ is recommended to
minimize the amount of segregated SrO. In order to
grown large crystals, the amount of molten material as
well as its composition should be kept constant. This is
difficult to achieve probably owing to the continuous
evaporation of RuO₂ and because of the low density of
the rods.
6. The crystals are then cleaved.
Because of the layered structure of Sr₂RuO₄, the
melt-grown samples can be cleaved easily, and single-
crystals may be obtained from the interior part of the
cylinder.
With this technique it is possible to grow a cylindrical
Sr₂RuO₄ crystal of about 5 mm diameter and 10 mm length.
Having prepared the single-crystal Sr₂RuO₄
substrate, the manufacture of the heterostructure of
FIG. 3 involves the following additional steps:
1. The substrate 2 is rinsed in acetone and propanol
and attached to the heater of the sputtering chamber
with silver paint, for example.
2. On the upper (001) surface of the Sr₂RuO₄
substrate 2, a superconducting film 3 of, for example, YBa₂
Cu₃O₇-δ is epitaxially grown by hollow cathode rf-
magnetron sputtering, wherein the value of δ is prefera-
bly kept equal to zero, but can be made as large as 1.
The sputter parameters used encompass a substrate
heating block temperature of 500°-750° C, a total pres-
Sure (Ar/O₂=2:1) of 0.854 mbar, a plasma discharge of
150-170 V and 450 mA, and an aftergrowth cooldown
in a=0.5 bar O₂ lasting for=1 hour. The thickness of the super-
conductor film 3 can finally be in the range of 1 to
1000 nm.
3. The same step is repeated for the lower (001)
surface of the Sr₂RuO₄ substrate 2 to form superconductor
layer 4.
4. Electrical contacts are then made in the form of
35 indium dots, silver paint, or metal pads, such as gold
pads 5 and 6, for example, on the superconductor layers
3 and 4, respectively.
The manufacture of the MISFET-structure 7 FIG. 4
involves the following steps additional to the prepara-
tion of the Sr₂RuO₄ substrate 9:
1. A (100)-oriented SrTiO₃ barrier layer 10 is epitax-
ially grown by reactive rf-magnetron sputtering at 67 Pa
in an O₂/Ar atmosphere at 850° C (temperature of
the sample holder) as an insulator on top of the 45
Sr₂RuO₄ substrate 9 and is polished down to the desired
final thickness.
2. On top of the thinned barrier layer 10, a supercon-
ductor film 8 (of YBa₂Cu₃O₇-δ, for example) with the
thickness s is sputtered.
3. Gold pads 11 and 12 are provided on top of the
superconductor layer 8 to form source and drain
contacts, respectively.
4. On the back side of the substrate 9, a gate electrode
13 in the form of a metal layer, such as a gold layer, for
example, is deposited.
5. Optionally, substrate 9 and gate electrode 13 may
be arranged on an insulating support layer 14, be it for
stability, as indicated in FIG. 5. Support layer 14 may
again consist of SrTiO₃ and be epitaxially grown by
reactive rf-magnetron sputtering. The thickness of this
layer can be freely chosen.
From the measurements taken with several sample
embodiments of the field-effect transistor in accordance
with FIGS. 4 and 5, it has been determined that the
operating gate voltage V₉ should be in the range be-
tween 0.1 and 50 V, preferably 5 V, the thickness s of
the superconducting film should be in the range be-
tween 1 and 30 nm, and the thickness t of the insulating
layer should be in the range between 3 and 100 nm.
In accordance with the invention, MISFET-type
heterostructures consisting of high-Tc superconduc-

tor/SrTiO₃/Sr₂RuO₄ multilayers may be made which
allow the application of electrical fields larger than 10⁶
V/cm to the superconducting films. In these devices,
electric field-effects generate changes in the channel
resistance. The high-Tc superconductor films have a
preferred thickness on the order of 10 nm and are oper-
ated with gate voltages well below 30 Volts. The chan-
nel resistivity changes can be attributed to equally strong
changes of the carrier density in the high-Tc
superconductor.
It should be noted that Sr₂RuO₄ can also be used in
the form of thin films for certain applications. Those
skilled in the art will understand that such films can be
made with any of the conventional methods, such as
electron beam evaporation, thermal evaporation, chem-
ical vapor deposition, metalorganic vapor deposition,
laser ablation, rf-magnetron sputtering, spinning-on,
molecular beam epitaxy, etc., for example.
While this invention has been described with respect
to plural embodiments thereof, it will be understood by
those with skill in the art that changes in the above
description or illustrations may be made with respect to
form or detail without departing from the spirit or
scope of the invention.
We claim:
1. A method for manufacturing superconducting cir-
cuit elements, comprising:
weighing and grinding a ratio of strontium carbonate
SrCO₃ and ruthenium dioxide RuO₂ to form pow-
der;
mixing the powder with water and pressing it to form
rods;
sintering the rods in air;
melting the rods in a floating zone melting process to
form a melt.
Growing crystal materials form the melt having cy-
lindrical shape with layers of strontium ruthenate
Sr₂RuO₄ along the axis of the cylindrical shape;
cleaving the melt-grown crystal materials of
Sr₂RuO₄ and certain single-crystal substrates having
defined crystallographic surfaces;
etopographically growing on at least one (001)-surface of
the Sr₂RuO₄ substrate a film of a high-Tc copper
oxide-based superconductor material, the thickness of
the superconductor film being in the range of 1
to 1000 nm;
depositing metal pads onto said superconductor film
to form electrical contacts; and
applying a metal pad to the surface of the substrate to
form an electrical contact.
2. A method for manufacturing superconducting cir-
cuit elements in accordance with claim 1, wherein said
high-Tc superconductor material is YBa₂Cu₃O₇-δ and
wherein 0≤δ≤1.
3. A method for manufacturing superconducting cir-
cuit elements in accordance with claim 1, further com-
prising:
etopographically growing a (100)-oriented SrTiO₃ barrier
layer onto said Sr₂RuO₄ substrate; and depositing a
high-Tc superconductor layer on said barrier layer.
4. A method for manufacturing superconducting cir-
cuit elements in accordance with claim 3, wherein said
high-Tc superconductor material is YBa₂Cu₃O₇-δ, and
wherein 0≤δ≤1.
5. A method for manufacturing superconducting circuit elements in accordance with claim 1, further comprising:

depositing on the surface of the Sr$_2$RuO$_4$ substrate facing away from said barrier layer an insulating support layer consisting of SrTiO$_3$ and having a thickness in the range of 100 to 1000 nm.

6. A method for manufacturing superconducting circuit element in accordance with claim 5, wherein said high-$T_c$ superconductor material is YBa$_2$Cu$_3$O$_{7-\delta}$, and wherein 0$\leq$\delta$\leq$1.

7. A method for manufacturing superconducting circuit elements in accordance with claim 1, wherein:

8. A method for manufacturing superconducting circuit element in accordance with claim 7, wherein said high-$T_c$ superconductor material is YBa$_2$Cu$_3$O$_{7-\delta}$, and wherein 0$\leq$\delta$\leq$1.

9. A method for manufacturing superconducting circuit elements in accordance with claim 1, wherein:

an excess of RuO$_2$ is used to obtain a molar ratio of 2:1 of SrCO$_3$ to RuO$_2$ informing said single crystal substrate.

10. A method for manufacturing superconducting circuit element in accordance with claim 9, wherein said high-$T_c$ superconductor material is YBa$_2$Cu$_3$O$_{7-\delta}$, and wherein 0$\leq$\delta$\leq$1.

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